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Leonard J Hope Esq
Merchant & Gould PC
P O Box 2903
Minneapolis, MN 55402-0903

EXAMINER	
KNOLL, CLIFFORD H	
ART UNIT	**PAPER NUMBER**
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,797	SIVERTSEN, CLAS	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, and 18-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan (US 6038624).

Regarding claim 1, Chan discloses the host controlling a state of the control line such that communication with the hard disk drive is supported while the at least one control line is in a first state (e.g., col. 5, lines 7-11), and communication with the hard disk drive is suspended while the at least one control line is in a second state (e.g., col. 5, lines 3-5); and an intermediate communications gateway disposed between said bus and the hard disk drive, said intermediate communications gateway being responsive to the state of the at least one control line in order to permit communication between said host and the hard disk drive while the at least one control line is in the first state and to

isolate the hard disk drive from said bus while the at least one control line is in the second state, wherein said host and said intermediate communications gateway cooperate to communicate data relating to the hard disk drive via said bus while the at least one control line is in the second state (e.g., col. 3, lines 45-47).

Regarding claim 2, Chan also discloses communicating data relating to the hard disk drive via at least one of the chip select, address and data lines while the at least one control line is in the second state (e.g., col. 4, lines 1-8).

Regarding claim 3, Chan also discloses signals to said intermediate communications gateway via said bus while the at least one control line is in the second state such that said intermediate communications gateway is capable of subsequently providing instructions to the hard disk drive in accordance with the control signals (e.g., col. 3, lines 45-47).

Regarding claim 4, Chan also discloses signals selected from the group consisting of power control signals, alarm signals, a reset signal and visual indicator signals (e.g., col. 5, lines 3-5).

Regarding claim 5, Chan also discloses provides status signals to said host via said bus while the at least one control line is in the second state in response to a query from said host regarding status of the hard disk drive (e.g., col. 5, lines 45-49).

Regarding claim 6, Chan also discloses wherein said intermediate communications gateway provides status signals selected from the group consisting of a drive presence signal, a failure signal, an alarm signal, a visual indicator status signal, a temperature signal and an operational state signal (e.g., col. 5, lines 45-49).

Regarding claim 7, Chan also discloses wherein said intermediate communications gateway supports local communication with the hard disk drive while the at least one control line is in the second state and the hard disk drive is isolated from said bus (e.g., col. 5, lines 45-49).

Regarding claim 8, Chan also discloses wherein said intermediate communications gateway continues to supply power to the hard disk drive while the at least one control line is in the second state and the hard disk drive is isolated from said bus (e.g., col. 5, lines 45-49).

Regarding claim 18, Chan discloses permitting communications between a host and the hard disk drive via a bus while at least one control line of the bus is in a first state (e.g., col. 5, lines 7-11); detecting a transition of the at least one control line from the first state to a second state; isolating the hard disk drive from the bus following detection of the transition and while the at least one control line remains in the second state (e.g., col. 5, lines 3-5); and communicating data relating to the hard disk drive via the bus between an intermediate communications gateway and the host while the at least one control line is in the second state and the hard disk drive is isolated from the bus (e.g., col. 5, lines 44-45).

Regarding claim 19, Chan also discloses the chip select, address and data lines, and wherein communicating data while the hard disk drive is isolated from the bus comprises communicating data relating to the hard disk drive between the host and the intermediate communications gateway via at least one of the chip select, address and data lines (e.g., col. 4, lines 1-8).

Regarding claim 20, Chan also discloses providing control signals from the host to the intermediate communications gateway via the bus, and wherein the method further comprises subsequently providing instructions from the intermediate communications gateway to the hard disk drive in accordance with the control signals (e.g., col. 5, lines 45-49).

Regarding claim 21, Chan also discloses providing control signals selected from the group consisting of power control signals, alarm signals, a reset signal and visual indicator signals (e.g., col. 5, lines 3-5).

Regarding claim 22, Chan also discloses while the hard disk drive is isolated from the bus comprises providing status signals from the intermediate communications gateway to the host via the bus in response to a query from the host regarding status of the hard disk drive (e.g., col. 5, lines 45-49).

Regarding claim 23, Chan also discloses wherein providing status signals comprises providing status signals selected from the group consisting of a drive presence signal, a failure signal, an alarm signal, a visual indicator status signal, a temperature signal and an operational state signal (e.g., col. 5, lines 45-49).

Regarding claim 24, Chan also discloses supporting local communications between the intermediate communications gateway and the hard disk drive while the at least one control line is in the second state and the hard disk drive is isolated from the bus (e.g., col. 5, lines 45-49).

Regarding claim 25, Chan also discloses continuing to supply power to the hard disk drive while the at least one control line is in the second state and the hard disk drive is isolated from the bus (e.g., col. 5, lines 45-49).

Claims 1-8, and 18-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakarda (US 6594721).

Regarding claim 1, Sakarda discloses the host controlling a state of the control line such that communication with the hard disk drive is supported while the at least one control line is in a first state (e.g., col. 8, lines 46-48), and communication with the hard disk drive is suspended while the at least one control line is in a second state (e.g., col. 5, lines 3-5); and an intermediate communications gateway disposed between said bus and the hard disk drive, said intermediate communications gateway being responsive to the state of the at least one control line in order to permit communication between said host and the hard disk drive while the at least one control line is in the first state and to isolate the hard disk drive from said bus while the at least one control line is in the second state, wherein said host and said intermediate communications gateway cooperate to communicate data relating to the hard disk drive via said bus while the at least one control line is in the second state (e.g., col. 12, lines 5-8).

Regarding claim 2, Sakarda also discloses communicating data relating to the hard disk drive via at least one of the chip select, address and data lines while the at least one control line is in the second state (e.g., col. 11, lines 15-20).

Regarding claim 3, Sakarda also discloses signals to said intermediate communications gateway via said bus while the at least one control line is in the second state such that said intermediate communications gateway is capable of subsequently providing instructions to the hard disk drive in accordance with the control signals (e.g., col. 12, lines 43-48).

Regarding claim 4, Sakarda also discloses signals selected from the group consisting of power control signals, alarm signals, a reset signal and visual indicator signals (e.g., col. 12, lines 54-59).

Regarding claim 5, Sakarda also discloses provides status signals to said host via said bus while the at least one control line is in the second state in response to a query from said host regarding status of the hard disk drive (e.g., col. 13, lines 2-9).

Regarding claim 6, Sakarda also discloses wherein said intermediate communications gateway provides status signals selected from the group consisting of a drive presence signal, a failure signal, an alarm signal, a visual indicator status signal, a temperature signal and an operational state signal (e.g., col. 13, lines 2-9).

Regarding claim 7, Sakarda also discloses wherein said intermediate communications gateway supports local communication with the hard disk drive while the at least one control line is in the second state and the hard disk drive is isolated from said bus (e.g., col. 13, lines 55-59).

Regarding claim 8, Sakarda also discloses wherein said intermediate communications gateway continues to supply power to the hard disk drive while the at

least one control line is in the second state and the hard disk drive is isolated from said bus (e.g., col. 12, lines 54-59).

Regarding claim 18, Sakarda discloses permitting communications between a host and the hard disk drive via a bus while at least one control line of the bus is in a first state (e.g., col. 8, lines 46-48); detecting a transition of the at least one control line from the first state to a second state; isolating the hard disk drive from the bus following detection of the transition and while the at least one control line remains in the second state (e.g., col. 5, lines 3-5); and communicating data relating to the hard disk drive via the bus between an intermediate communications gateway and the host while the at least one control line is in the second state and the hard disk drive is isolated from the bus (e.g., col. 12, lines 5-8).

Regarding claim 19, Sakarda also discloses the chip select, address and data lines, and wherein communicating data while the hard disk drive is isolated from the bus comprises communicating data relating to the hard disk drive between the host and the intermediate communications gateway via at least one of the chip select, address and data lines (e.g., col. 12, lines 54-59).

Regarding claim 20, Sakarda also discloses providing control signals from the host to the intermediate communications gateway via the bus, and wherein the method further comprises subsequently providing instructions from the intermediate communications gateway to the hard disk drive in accordance with the control signals (e.g., col. 12, lines 43-48).

Regarding claim 21, Sakarda also discloses providing control signals selected from the group consisting of power control signals, alarm signals, a reset signal and visual indicator signals (e.g., col. 13, lines 55-59).

Regarding claim 22, Sakarda also discloses while the hard disk drive is isolated from the bus comprises providing status signals from the intermediate communications gateway to the host via the bus in response to a query from the host regarding status of the hard disk drive (e.g., col. 13, lines 2-9).

Regarding claim 23, Sakarda also discloses wherein providing status signals comprises providing status signals selected from the group consisting of a drive presence signal, a failure signal, an alarm signal, a visual indicator status signal, a temperature signal and an operational state signal (e.g., col. 12, lines 54-59).

Regarding claim 24, Sakarda also discloses supporting local communications between the intermediate communications gateway and the hard disk drive while the at least one control line is in the second state and the hard disk drive is isolated from the bus (e.g., col. 12, lines 54-59).

Regarding claim 25, Sakarda also discloses continuing to supply power to the hard disk drive while the at least one control line is in the second state and the hard disk drive is isolated from the bus (e.g., col. 12, lines 54-59).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-17, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan in view of widely used standard system bus embodiments, as further evidenced by Lichtman (US 5787246).

Regarding claim 9, Chan also discloses a standard system bus and a RESET line in his particular embodiment but fails to mention such standard precursors to his system bus such as the AT bus; however Examiner takes Official Notice that the AT bus is a widely-known and practiced bus standard for communicating with IDE devices such as the invention of Chan. This is further evidenced by Lichtman, who discloses device configuration for a system bus and discloses the equivalence, for such purpose of the standard system buses that are commonly used to configure devices (e.g., col. 3, lines 54-67, "ISA", "PCI"). It would be obvious to combine a standard precursor system bus such as the AT bus with Chan, because the AT bus and its control, address and data signals are widely known to have equivalent use in device control such as in the invention of Chan. Therefore it would be obvious to one of ordinary skill in the art to

combine the standard system AT bus with the computer system of Chan to obtain the claimed invention.

Regarding claim 10, Chan discloses a system bus having a plurality of lines including a RESET line an IDE hard disk drive capable of communicating via the system bus (e.g., col. 3, lines 13-15); a host for communicating via the system bus with said IDE hard disk drive, said host capable of alternately asserting and deasserting the RESET line; and an intermediate communications gateway disposed between said system bus and said IDE hard disk drive, said intermediate communications gateway being responsive to the RESET line in order to permit communication between said host and said IDE hard disk drive while the RESET line is deasserted (e.g., col. 5, lines 7-11) and to isolate said IDE hard disk drive from said system bus while the RESET line is asserted (e.g., col. 5, lines 3-5), wherein said host and said intermediate communications gateway cooperate to communicate data relating to said IDE hard disk drive via the system bus while the RESET line is asserted (e.g., col. 3, lines 45-47). Chan also discloses a standard system bus and a RESET line in his particular embodiment but fails to mention such standard precursors as the AT bus; however Examiner takes Official Notice that the AT bus is a widely-known and practiced bus standard for communicating with IDE devices such as the invention of Chan. This is further evidenced by Lichtman, who discloses device configuration for a system bus and discloses the equivalence, for that purpose of the standard system buses that are commonly used to configure IDE devices (e.g., col. 3, lines 54-67, "ISA", "PCI"). It would be obvious to combine a standard precursor system bus such as the AT bus with

Chan, because the AT bus and its control, address and data signals are widely known to have equivalent use in device control such as in the invention of Chan. Therefore it would be obvious to one of ordinary skill in the art to combine the standard system AT bus with the computer system of Chan to obtain the claimed invention.

Regarding claim 11, Chan also discloses chip select, address and data lines, and wherein said host and said intermediate communications gateway communicate data relating to said IDE hard disk drive via at least one of the chip select, address and data lines while the RESET line is asserted (e.g., col. 4, lines 1-8).

Regarding claim 12, Chan also discloses host provides control signals to said intermediate communications gateway via the system bus while the RESET line is asserted such that said intermediate communications gateway is capable of subsequently providing instructions to said IDE hard disk drive in accordance with the control signals (e.g., col. 3, lines 45-47).

Regarding claim 13, Chan also discloses the signals selected from the group consisting of power control signals, alarm signals, a reset signal and visual indicator signals (e.g., col. 5, lines 3-5).

Regarding claim 14, Chan also discloses the intermediate communications gateway provides status signals to said host via said system bus while the RESET line is asserted in response to a query from said host regarding status of said IDE hard disk drive (e.g., col. 5, lines 45-49).

Regarding claim 15, Chan also discloses the intermediate communications gateway provides status signals selected from the group consisting of a drive presence

signal, a failure signal, an alarm signal, a visual indicator status signal, a temperature signal and an operational state signal (e.g., col. 5, lines 45-49).

Regarding claim 16, Chan also discloses the intermediate communications gateway supports local communication with said IDE hard disk drive while the RESET line is asserted and said IDE hard disk drive is isolated from the system bus (e.g., col. 5, lines 45-49).

Regarding claim 17, Chan also discloses the intermediate communications gateway continues to supply power to said IDE hard disk drive while the RESET line is asserted and said IDE hard disk drive is isolated from said system bus (e.g., col. 5, lines 45-49).

Regarding claim 26, Chan also discloses a standard system bus and a RESET line transition detection in his particular embodiment (e.g., col. 3, lines 33-35) but fails to mention such standard precursors to his system bus such as the AT bus; however Examiner takes Official Notice that the AT bus is a widely-known and practiced bus standard for communicating with IDE devices such as the invention of Chan. This is further evidenced by Lichtman, who discloses device configuration for a system bus and discloses the equivalence, for that purpose of the standard system buses that are commonly used to configure IDE devices (e.g., col. 3, lines 54-67, "ISA", "PCI"). It would be obvious to combine a standard precursor system bus such as the AT bus with Chan, because the AT bus and its control, address and data signals are widely known to have equivalent use in device control such as in the invention of Chan. Therefore it

would be obvious to one of ordinary skill in the art to combine the standard system AT bus with the computer system of Chan to obtain the claimed invention.

Claims 9-17, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakarda in view of widely used standard system bus embodiments, as further evidenced by Lichtman.

Regarding claim 9, Sakarda also discloses a standard system bus and a RESET line in his particular embodiment and briefly notes legacy support for precursor buses (e.g., col. 8, lines 44-48), but fails to mention such standard precursors to his system bus such as the AT bus to practice his invention; however Examiner takes Official Notice that the AT bus is a widely-known bus standard for communicating with IDE devices such as the invention of Sakarda. This is further evidenced by Lichtman, who discloses device configuration for a system bus and discloses the equivalence, for such purpose of the standard system buses that are commonly used to configure devices (e.g., col. 3, lines 54-67, "ISA", "PCI"). It would be obvious to combine a standard precursor system bus such as the AT bus with Sakarda, because the AT bus and its control, address and data signals are widely known to have equivalent use in device control such as in the invention of Sakarda. Therefore it would be obvious to one of ordinary skill in the art to combine the standard system AT bus with the computer system of Sakarda to obtain the claimed invention.

Regarding claim 10, Sakarda discloses a system bus having a plurality of lines including a RESET line an IDE hard disk drive capable of communicating via the system bus (e.g., col. 8, lines 46-48); a host for communicating via the system bus with said IDE hard disk drive, said host capable of alternately asserting and deasserting the RESET line; and an intermediate communications gateway disposed between the system bus and said IDE hard disk drive, said intermediate communications gateway being responsive to the RESET line in order to permit communication between said host and said IDE hard disk drive while the RESET line is deasserted (e.g., col. 8, lines 46-48) and to isolate said IDE hard disk drive from said system bus while the RESET line is asserted (e.g., col. 5, lines 3-5), wherein said host and said intermediate communications gateway cooperate to communicate data relating to said IDE hard disk drive via the system bus while the RESET line is asserted (e.g., col. 11, lines 15-20). Sakarda also discloses a standard system bus and a RESET line in his particular embodiment and briefly notes legacy support for precursor buses (e.g., col. 8, lines 44-48), but fails to mention such standard precursors to his system bus such as the AT bus to practice his invention; however Examiner takes Official Notice that the AT bus is a widely-known bus standard for communicating with IDE devices such as the invention of Sakarda. This is further evidenced by Lichtman, who discloses device configuration for a system bus and discloses the equivalence, for such purpose of the standard system buses that are commonly used to configure devices (e.g., col. 3, lines 54-67, "ISA", "PCI"). It would be obvious to combine a standard precursor system bus such as the AT bus with Sakarda, because the AT bus and its control, address and data signals are

widely known to have equivalent use in device control such as in the invention of Sakarda. Therefore it would be obvious to one of ordinary skill in the art to combine the standard system AT bus with the computer system of Sakarda to obtain the claimed invention.

Regarding claim 11, Sakarda also discloses chip select, address and data lines, and wherein said host and said intermediate communications gateway communicate data relating to said IDE hard disk drive via at least one of the chip select, address and data lines while the RESET line is asserted (e.g., col. 11, lines 15-20).

Regarding claim 12, Sakarda also discloses host provides control signals to said intermediate communications gateway via the system bus while the RESET line is asserted such that said intermediate communications gateway is capable of subsequently providing instructions to said IDE hard disk drive in accordance with the control signals (e.g., col. 12, lines 43-48).

Regarding claim 13, Sakarda also discloses the signals selected from the group consisting of power control signals, alarm signals, a reset signal and visual indicator signals (e.g., col. 12, lines 54-59).

Regarding claim 14, Sakarda also discloses the intermediate communications gateway provides status signals to said host via said system bus while the RESET line is asserted in response to a query from said host regarding status of said IDE hard disk drive (e.g., col. 13, lines 2-9).

Regarding claim 15, Sakarda also discloses the intermediate communications gateway provides status signals selected from the group consisting of a drive presence

signal, a failure signal, an alarm signal, a visual indicator status signal, a temperature signal and an operational state signal (e.g., col. 13, lines 2-9).

Regarding claim 16, Sakarda also discloses the intermediate communications gateway supports local communication with said IDE hard disk drive while the RESET line is asserted and said IDE hard disk drive is isolated from the system bus (e.g., col. 13, lines 55-59).

Regarding claim 17, Sakarda also discloses the intermediate communications gateway continues to supply power to said IDE hard disk drive while the RESET line is asserted and said IDE hard disk drive is isolated from said system bus (e.g., col. 12, lines 54-59).

Regarding claim 26, Sakarda also discloses a standard system bus and a RESET line transition detection in his particular embodiment (e.g., col. 9, lines 5-6), and also discloses a standard system bus and a RESET line in his particular embodiment and briefly notes legacy support for precursor buses (e.g., col. 8, lines 44-48), but fails to mention such standard precursors to his system bus such as the AT bus to practice his invention; however Examiner takes Official Notice that the AT bus is a widely-known bus standard for communicating with IDE devices such as the invention of Sakarda. This is further evidenced by Lichtman, who discloses device configuration for a system bus and discloses the equivalence, for such purpose of the standard system buses that are commonly used to configure devices (e.g., col. 3, lines 54-67, "ISA", "PCI"). It would be obvious to combine a standard precursor system bus such as the AT bus with Sakarda, because the AT bus and its control, address and data signals are widely

known to have equivalent use in device control such as in the invention of Sakarda. Therefore it would be obvious to one of ordinary skill in the art to combine the standard system AT bus with the computer system of Sakarda to obtain the claimed invention.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Deschepper (US 6145029) also discloses an embodiment of a control line and intermediate gateway to responsively communicate with or isolate the hard disk.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100